SPECIFICATIONS

GENERAL

ADC Type: Gated Current-Integrating, 12 bits.
Signal Inputs: 96 input channels. Quasi-differential. Impedance 50 Ω on each of the 2 input pins belonging to one channel; 100 Ω differential. Protected to ±100 V for 1 μsec.
Signal Input Connector: Six 34-pin headers on front panel.
Gate Input: Differential ECL input via a 2-pin front-panel connector or TR1 (B47) and TR2 (B48) lines on the FASTBUS backplane. May be driven by the Model 1810 CAT Module. The front-panel input uses removable termination resistors for busing of more than one module; 50 nsec to 2 μsec.[1] ***Caution:*** at lower gate widths the peak signal currents may conflict with linearity and/or full scale specifications.
Common Mode Rejection Ratio: > 50 dB for ±200 mV DC to 1 kHz.[1]
Conversion In Progress (CIP) Output: Front-panel output to indicate an A-to-D conversion is occurring. ECL signal on 2-pin header.
Fast Clear: Differential ECL input via a 2-pin front-panel connector or backplane T0 line. Clears module and readies it for a new Gate. For channel occupancy less than 50%, ADC results settle to within ±2 counts in less than 600 nsec. For higher occupancy, clearing time is 950 nsec.
Fast Analog Output: 24 ungated current sum signals on Auxiliary FASTBUS connector. Signal shape same as analog input; signal amplitude = 0.1 times input signal amplitude. Output impedance: ≥ 100 kΩ. Output compliance: 4 to 7 V.
Test Conditions for Following Specifications: (Unless otherwise stated.)

1. 25 pC input.
2. FASTBUS crate occupied by one Model 1821 SM/I, one 1810 CAT and one unit under test.
3. 1.5 μsec gate width.
4. 10 μsec MPI.

Pedestal: 300 ±200 counts. Pedestal spread is reduced with narrower gates. Adjustable with an on-board trim pot.
Full Scale Charge: Low range, 170 pC[1]; high range 1350 pC[1].
Sensitivity: Low range, 50 fC/count ±3%; high range 400 fC/count ±5%.
Integral Linearity: Low range < ±(0.25% of reading + 2 counts); high range < ±0.50% of reading + 2 counts.
Differential Non-Linearity: ±30% typical, -0.75 LSB to +1.25 LSB maximum, see manual for details.
Operating Region: +10 mV to -1.5 V for specified linearity, (+0.2 mA to -30 mA into 50 Ω).[1]
Noise: 0.8 counts R.M.S. typical, 2 counts maximum. Tested with no signals connected and a constant conversion rate.
Interchannel Isolation: 75 dB typical, 60 dB minimum.[1]
Temperature Coefficient: < ±(0.1% of reading + 1 count)/C (inputs unconnected or driven by a high impedance source).[1]
Long Term Stability: ±(0.25% of reading + 1 count)/week.[1]
Rate Effect: (Variation in pedestal with gate-clear repetition rate). Board average: 1.5 counts typical 2.5 counts max. Individual channel: board average ±1.5 counts.[2]
Conversion Time: 265 μsec for all 96 channels. Subtract 2.7 μsec per channel if less than 96 channels are programmed for data taking.
Multiple Event Buffer: The digital data memory is large enough to store the results of up to eight events (8 times 96 A-to-D conversions). A 3-bit event counter allows the user to keep track of how many events the readout is trailing the A-to-D conversion.
Measure Pause Interval: 2 μsec to 300 μsec.[1] Less than 2 μsec permitted, but a degradation of performance on channel 0 may occur.
Calibration Feature: Allows the gain of any channel to be measured to within ±1.5%. Needs an external DC voltage and a Gate signal. The charge pulse applied to all channels is proportional to the DC voltage across the differential Test Level Inputs on the FASTBUS backplane.
Voltage Range: 0 to 10 V. The calibration coefficient is 160 pC/V.
Packaging: Single-width FASTBUS module (ANSI/IEEE 960-1986).
Power Requirements: 600 mA at +15 V; 3.1 A at +5 V; 400 mA at -2 V; 2.1 A at -5.2 V; 100 mA at -15 V (37.7 W total).

FASTBUS CONTROL

Addressing Modes: Geographic, and Broadcast (cases 1, 3, 4, 7). Implemented Registers: CSR0, CSR1, DSR0 (FIFO).
Module Identification Code: $(1045)_h$.
Slave Status Responses to Data Cycles:

SS	*Significance*
0	Valid Action
1	Busy
2	End of Data
6	Error. Invalid Mode
7	Error. Invalid Secondary Address loaded into internal address register.

[1] Guaranteed by design. Not tested.
[2] Sample tested.

Implemented Broadcast Functions:

Code	*Significance*	*Comments*
01_h	General Broadcast Select	The ADC modules are selected and respond to subsequent data cycles.
09_h	Sparse Data Scan	ADC modules containing data assert the T pin on the following read data cycle.
09_h	Pattern Select	ADCs, seeing their T pin asserted on the following write data cycle, become selected to respond to subsequent data cycle.
$0D_h$	All Device Scan	All ADC modules assert their T pin on the following read data cycle.
$9D_h$	ADC SDS	Unique Sparse Data Scan for 1880 Series modules only. Follows standard SDS (see above).
CD_h	Personality Card SDS	Sparse Data Scan: ADC asserts T pin if Personality Card requires service.

An h subscript indicates hexadecimal (base 16).

FASTBUS REGISTER CONFIGURATIONS

CSR 0 Write Bit Definitions